規格書
DataSheet

CUSTOMER :

Company Name

Allied Vision

Model NO :

FWX2-PCIE10

DESCRIPTION :

Dual OHCI 1.1 Compliant FireWire to PCI Express Host Adapters

Revision :

1.1.0

CUSTOMER APPROVED	APPROVAL	ENGINNER	ISSUE BY

IOI Technology Corporation
映奧股份有限公司
台北縣新店市寶橋路235巷125號4樓
4F, No.125, Lane 235, Pao Chiao Road,
Hsin Tian City, Taipei, Taiwan, R.O.C.
TEL : 02-89191358 FAX : 02-89191359

Contents

FWx2-PCIE10 Overview

Introduction:

The FWx2-PCIE10 is a dual OHCI 1.1 Compliant FireWire (IEEE 1394a) to PCI Express Host Adapter. FWx2-PCIE10 is designed with two key components.

- PCI Express to PCI Bus Translation bridge.
- OHCI 1.1 Compliant IEEE 1394a Single Chip Host Controller.

The PCI Express to PCI local bus translation bridge takes advantages of the 2.5 Gb/s burst rate of 1-lane PCI Express bus and the PCI bus interface is connected to two OHCI 1.1 Compliant IEEE 1394a Single Chip Host Controller (TSB43AB22A). This solution provides full PCI Express and dual 1394a functionality and performance.

Application:

1. Multi-DV Camera:

FWx2-PCIE10 is aimed at higher-speed multi-DV camera application. You can bring the video or image from multi-DV camera directly into your computer over a IEEE-1394 connection as a perfect digital copy, with no conversion losses.

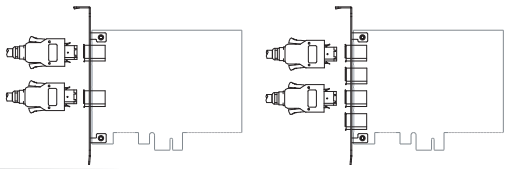
2. Storage:

FWx2-PCIE10 delivers the performance and connectivity required for I/O demanding applications such as CD-ROM servers, Video-On-Demand, database servers, workstations, high-end desktops, software RAID sub systems, and image systems.

3. Networks:

IP Over 1394 is an innovative software networking solution which provides High Speed LAN at 400Mbps, and it beats the Fastest available alternatives Hands Down (Fast Ethernet 100Mbps).

Support Two FireWire Plug w/Latch type Cable



Specification:

PCI Express and PCI:	- Supports 1-lane 2.5 Gb/s PCI Express. - Utilizes 100-MHz Differential PCI Express Common Reference Clock - Fully Compliant with PCI Express Base Specification, Revision 1.0a - Packetized serial traffic with PCI Express split completion protocol - Automatic retry of bad packets - 8b/10b signal encoding - In-band interrupts and messages - Support of message signaled interrupts - Fully Compliant with PCI Local Bus Specification, Revision 3.0 - PCI Bus Power Management Interface r1.1 Compliant
IEEE 1394 Std Support:	- Fully compliant with provisions of IEEE Std 1394-1995 for high-performance serial bus and the IEEE Std 1394a-2000. - Fully Compliant with 1394 Open Host Controller Interface Specification, Revision 1.1. - Full IEEE Std 1394a-2000 Support Includes: Connection Debounce, Arbitrated Short Reset, Multispeed Concatenation, Arbitration Acceleration, Fly-by Concatenation, and Port Disable/Suspend/Resume. - EEPROM Configuration Support to Load the Global Unique ID for the 1394 Fabric
1394 Bus Transfer Rate:	IEEE Std 1394a-2000 Fully Compliant Cable Ports at 100M Bits/s, 200M Bits/s, and 400M Bits/s.
Number of Ports:	FWx2-PCIE10-2: Two FireWire P1394a Cable Ports * OHCI 1 (FW-6pin X 1) * OHCI 2 (FW-6pin X 1) FWx2-PCIE10-4: Four FireWire P1394a Cable Ports * OHCI 1 (FW-6pin X 2) * OHCI 2 (FW-6pin X 2)
Power Management:	D0, D1, D2, and D3 power states and PME events per the PCI Bus Power Management Interface Specification
Bus Power Connector:	Big IDE 4-pin DC Power Connector

RoHS:

This Host Adapter is satisfied with RoHS regulations. Material of solder is satisfied with following definition.

	Material of solder
Solder Paste	SN-3.0AG-0.5CU
Flow and hand soldering	SN-0.7CU+NI

Environmental Condition:

Operating free-air temperature: 0 ~ 65 degree C
Storage temperature range: -20 ~ 100 degree C
Humidity Operating : 0 ~ 80% RH, Non-condensing

IEEE 1394 Power Class:

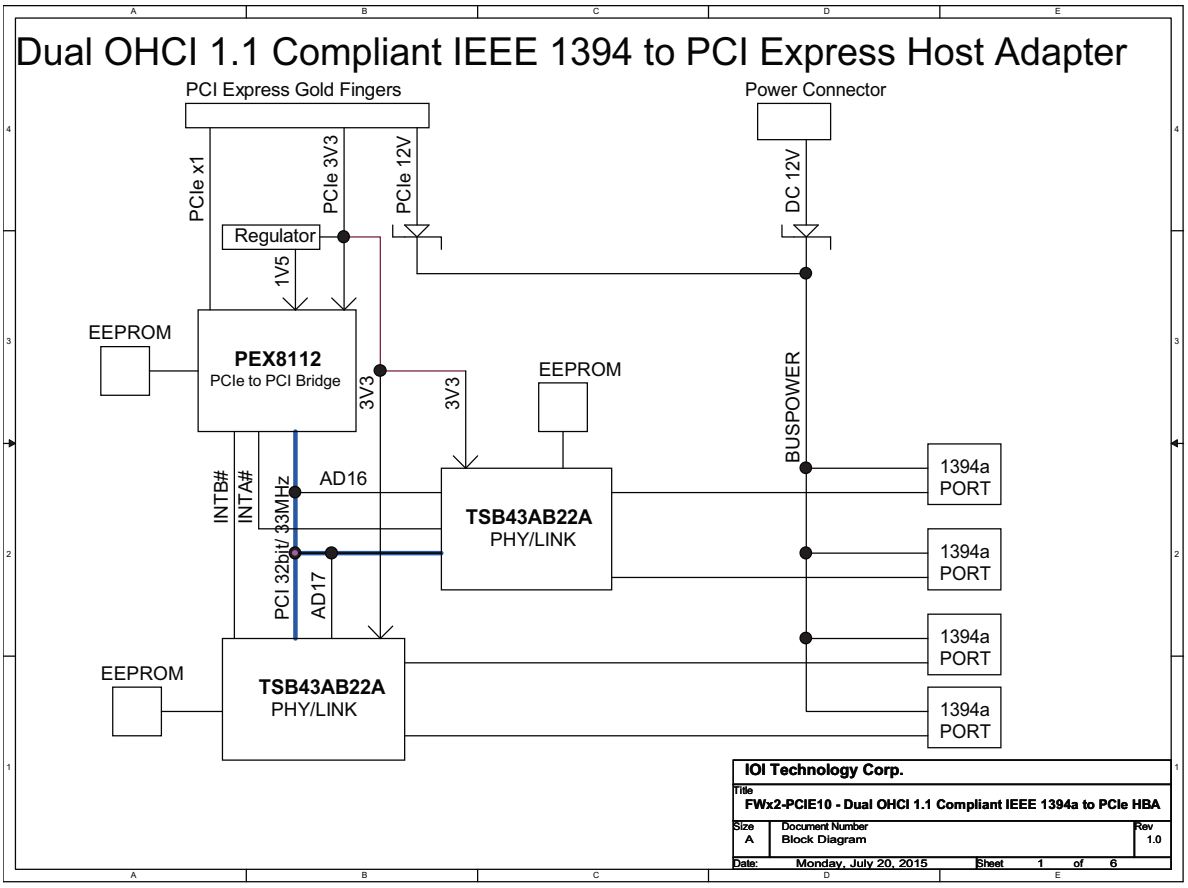
FWx2-PCIE10 was designed with 1394 power class 1 (PC0 ~ PC2 = 001).
FWx2-PCIE10 is a self-powered device and provides a minimum of 15W to the bus.
Power Class Descriptions

PC0 ~ PC2	DESCRIPTION
001	Node is self-powered and provides a minimum of 15 W to the bus.

IEEE 1394 Bus Power:

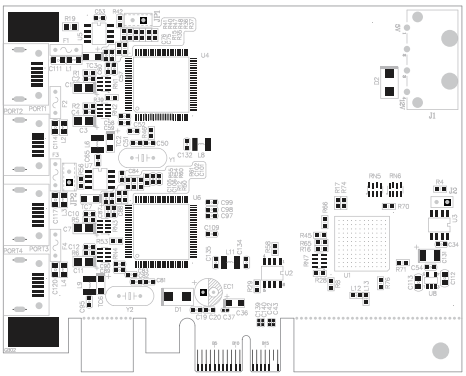
Power supply to the FireWire (IEEE 1394) bus power may from the following source
A. From PCI Express: +12V (500mA)
B. From J1: SMPS (Switching Mode Power Supply) DC +12V
C. From FireWire (IEEE 1394) Bus Power
*IEEE 1394 Bus Power (Power for the IEEE 1394 Bus): All FireWire (IEEE 1394) port is protected by one 1.35A/33V Fuse.

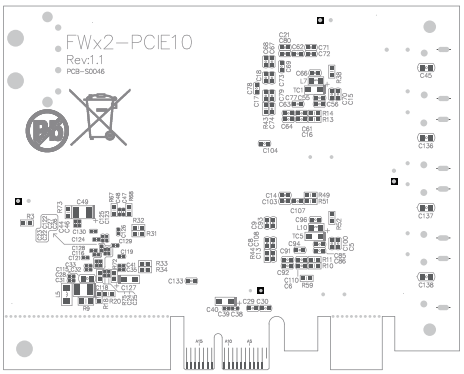
Block Diagram :



Silk Screen and Pictures

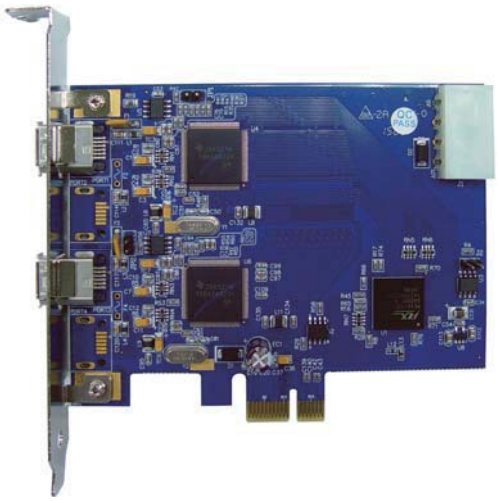
Silk Screen of FWX2-PCIE10 P.C.B. :





Picture of FWX2-PCIE10 PCBA:

FWX2-PCIE10-2



Top View

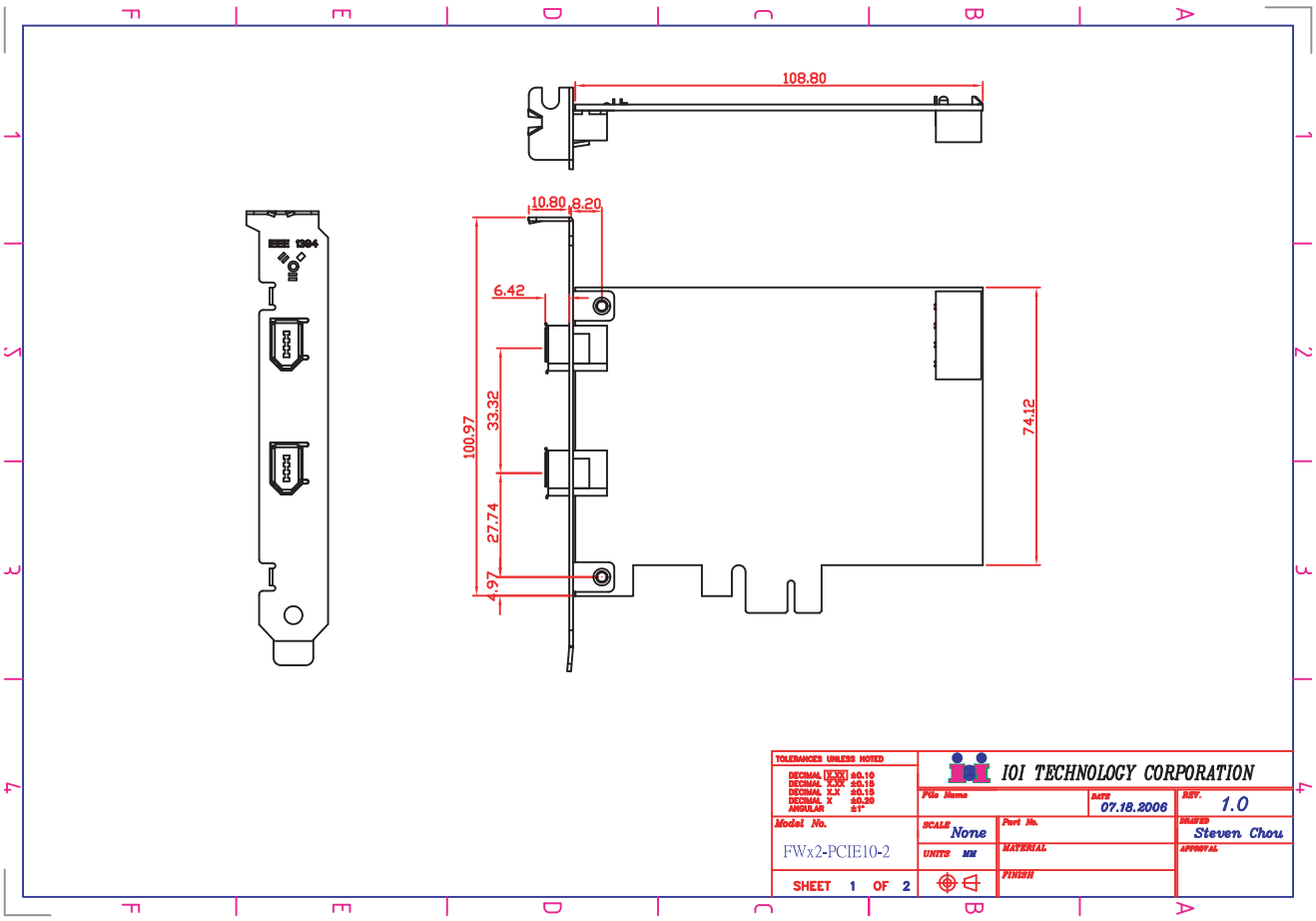
Bottom View

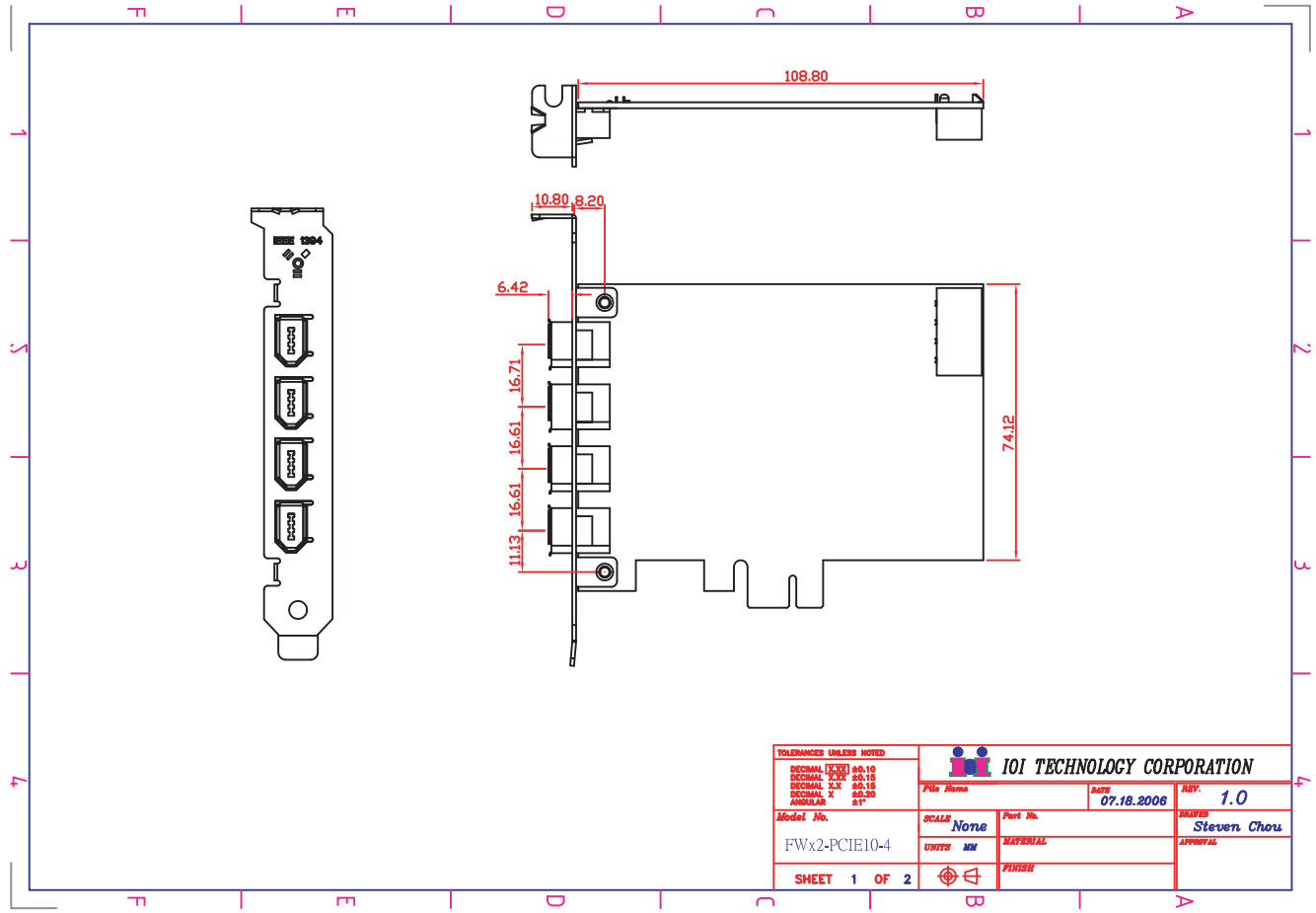
FWX2-PCIE10-4

Top View

Bottom View

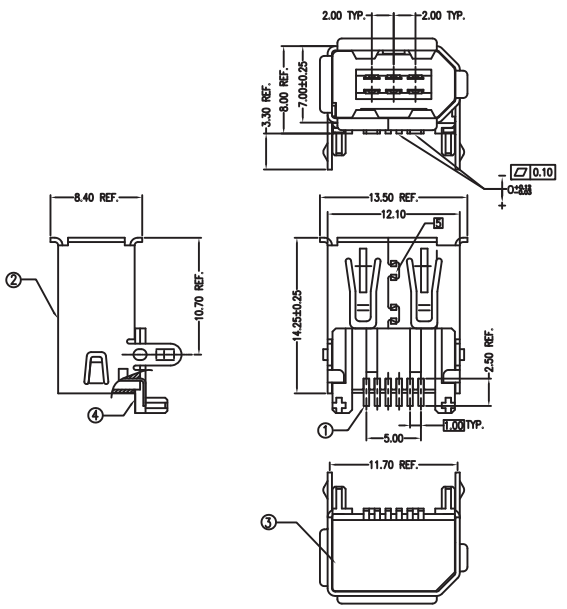
Mechanical Dimension

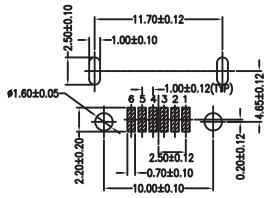




Datasheet of FireWire Connector

REV	DATE	REMARK





RECOMMENDED PCB LAYOUT(t=1.60±0.15)
COMPONENT SIDE

NOTE:
AF2**006KO

- HOUSING COLOR
  - S: BLACK
  - 1: WHITE
  - T: BEIGE
  - 7: GRAY
- FORNT SHELL PLATING
  - J: Ni 40u"
  - N: G/F, OVER Ni 40u"

5 GAP: 0.25mm(Max).

ITEM	DESC.	MATERIAL	REMARKS	PART REMARKS
4	HOUSING	HIGH TEMPERATURE THERMOPLASTICS	30%G.F. UL94V-0 COLOR:SEE NOTE	
3	REAR SHELL	STEEL (T=0.30)	OVER PLATING: Ni100u"	
2	FRONT SHELL	COPPER ALLOY (T=0.40)	OVER PLATING:SEE NOTE	
1	TERMINAL	COPPER ALLOY(T=0.20)	CONTACT AREA: Au30u" SOLDER AREA: Sn100u" UNDER PLATING: Ni50u"	

TOLERANCES UNLESS NOTED

DECIMAL	XXX	±0.10
DECIMAL	X.XX	±0.15
DECIMAL	X.X	±0.15
DECIMAL	X	±0.20
ANGULAR		±1°

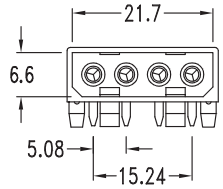
IOI TECHNOLOGY CORPORATION

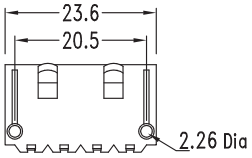
File Name: CO-M0015-02		Date	Rev: 1.0
Model No.: CO-M0015-02	Scale: NONE	Part No.: CO-M0015-02	Drawed
	Units: m m	Material: NONE	Approval
Sheet 1 of 2		Finish: NONE	A4

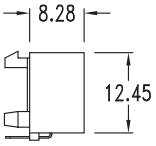
REV	DATE	REMARK

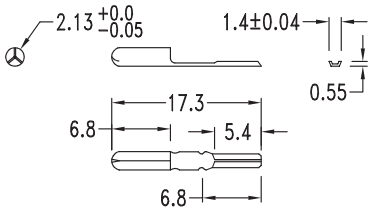
Features/Specifications:

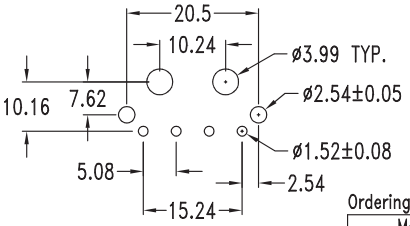
- UL 94V-2 nylon 66, Natural color
- Pins: Phosphor bronze Thickness 0.25mm
- Plating tin
- Two P.C tail lengths
- Voltage Rating: 250V AC (R.M.S)
- Current Rating: 6.5 amperes
- Dielectric Withstanding Voltage: 1500 VAC for 60 sec.
- Insulation Resistance: 500 megohms milliohms
- Contact Resistance: 10 milliohms maximun
- Ambient Temperature Range: -40°C to 105°C

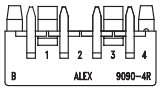












Ordering Information

Model No.	P.C Tail Lengtb
CO-M0019	3.6±0.5mm

TOLERANCES UNLESS NOTED DECIMAL XXX ±0.10 DECIMAL XX ±0.15 DECIMAL X.X ±0.15 DECIMAL X ±0.20 ANGULAR ±1°	IOI TECHNOLOGY CORPORATION		
	File Name CO-M0019	Date	Rev 1.0
Model No. CO-M0019	Scale NONE	Part No. CO-M0019	Drawed V-0431
	Units m m	Material NONE	Approval
Sheet 1 of 1		Finish NONE	A4

TEXAS INSTRUMENTS

TSB43AB22A

Integrated 1394a-2000 OHCI PHY/Link-Layer Controller

Data Manual

NOTE **Designing with this device may require extensive support. Before incorporating this device into a design, customers should contact TI or an Authorized TI Distributor.**

December 2001 *1394 Host Controller Solutions*

SLLS520

1 Introduction

This chapter provides an overview of the Texas Instruments TSB43AB22A device and its features.

1.1 Description

The Texas Instruments TSB43AB22A device is an integrated 1394a-2000 OHCI PHY/link-layer controller (LLC) device that is fully compliant with the *PCI Local Bus Specification*, the *PCI Bus Power Management Interface Specification*, IEEE Std 1394-1995, IEEE Std 1394a-2000, and the *1394 Open Host Controller Interface Specification*. It is capable of transferring data between the 33-MHz PCI bus and the 1394 bus at 100M bits/s, 200M bits/s, and 400M bits/s. The TSB43AB22A device provides two 1394 ports that have separate cable bias (TPBIAS). The TSB43AB22A device also supports the IEEE Std 1394a-2000 power-down features for battery-operated applications and arbitration enhancements.

As required by the *1394 Open Host Controller Interface Specification* (OHCI) and IEEE Std 1394a-2000, internal control registers are memory-mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles specified by PCI, and it provides plug-and-play (PnP) compatibility. Furthermore, the TSB43AB22A device is compliant with the *PCI Bus Power Management Interface Specification* as specified by the *PC 2001 Design Guide* requirements. The TSB43AB22A device supports the D0, D1, D2, and D3 power states.

The TSB43AB22A design provides PCI bus master bursting, and it is capable of transferring a cacheline of data at 132M bytes/s after connection to the memory controller. Because PCI latency can be large, deep FIFOs are provided to buffer the 1394 data.

The TSB43AB22A device provides physical write posting buffers and a highly-tuned physical data path for SBP-2 performance. The TSB43AB22A device also provides multiple isochronous contexts, multiple cacheline burst transfers, advanced internal arbitration, and bus-holding buffers.

An advanced CMOS process achieves low power consumption and allows the TSB43AB22A device to operate at PCI clock rates up to 33 MHz.

The TSB43AB22A PHY-layer provides the digital and analog transceiver functions needed to implement a two-port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

The TSB43AB22A PHY-layer requires only an external 24.576-MHz crystal as a reference for the cable ports. An external clock may be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216-MHz reference signal. This reference signal is internally divided to provide the clock signals that control transmission of the outbound encoded strobe and data information. A 49.152-MHz clock signal is supplied to the integrated LLC for synchronization and is used for resynchronization of the received data.

Data bits to be transmitted through the cable ports are received from the integrated LLC and are latched internally in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304M, 196.608M, or 393.216M bits/s (referred to as S100, S200, or S400 speeds, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the twisted-pair B (TPB) cable pair(s), and the encoded strobe information is transmitted differentially on the twisted-pair A (TPA) cable pair(s).

During packet reception, the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are resynchronized to the local 49.152-MHz system clock and sent to the integrated LLC. The received data is also transmitted (repeated) on the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage.

The TSB43AB22A device provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY layer contains two independent TPBIAS circuits. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1.0 μF.

The line drivers in the TSB43AB22A device operate in a high-impedance current mode and are designed to work with external 112-Ω line-termination resistor networks in order to match the 110-Ω cable impedance. One network is provided at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the TPA terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the TPB terminals is coupled to ground through a parallel R-C network with recommended values of 5 kΩ and 220 pF. The values of the external line-termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. An external resistor connected between the R0 and R1 terminals sets the driver output current and other internal operating currents. This current-setting resistor has a value of 6.34 kΩ ±1%.

When the power supply of the TSB43AB22A device is off and the twisted-pair cables are connected, the TSB43AB22A transmitter and receiver circuitry present a high impedance to the cable and do not load the TPBIAS voltage at the other end of the cable.

When the device is in a low-power state (for example, D2 or D3) the TSB43AB22A device automatically enters a low-power mode if all ports are inactive (disconnected, disabled, or suspended). In this low-power mode, the TSB43AB22A device disables its internal clock generators and also disables various voltage and current reference circuits, depending on the state of the ports (some reference circuitry must remain active in order to detect new cable connections, disconnections, or incoming TPBIAS, for example). The lowest power consumption (the ultralow-power sleep mode) is attained when all ports are either disconnected or disabled with the port interrupt enable bit cleared.

The TSB43AB22A device exits the low-power mode when bit 19 (LPS) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1 or when a port event occurs which requires that the TSB43AB22A device to become active in order to respond to the event or to notify the LLC of the event (for example, incoming bias is detected on a suspended port, a disconnection is detected on a suspended port, or a new connection is detected on a nondisabled port). When the TSB43AB22A device is in the low-power mode, the internal 49.153-MHz clock becomes active (and the integrated PHY layer becomes operative) within 2 ms after bit 19 (LPS) in the host controller control register at OHCI offset 50h/54h (see Section 4.16, *Host Controller Control Register*) is set to 1.

The TSB43AB22A device supports hardware enhancements to better support digital video (DV) and MPEG data stream reception and transmission. These enhancements are enabled through the isochronous receive digital video enhancements register at OHCI offset A88h (see Chapter 5, *TI Extension Registers*). The enhancements include automatic timestamp insertion for transmitted DV and MPEG-formatted streams and common isochronous packet (CIP) header stripping for received DV streams.

The CIP format is defined by the IEC 61883-1:1998 specification. The enhancements to the isochronous data contexts are implemented as hardware support for the synchronization timestamp for both DV and MPEG CIP formats. The TSB43AB22A device supports modification of the synchronization timestamp field to ensure that the value inserted via software is not stale—that is, the value is less than the current cycle timer when the packet is transmitted.

1.2 Features

The TSB43AB22A device supports the following features:

- Fully compliant with provisions of IEEE Std 1394-1995 for a high-performance serial bus† and IEEE Std 1394a-2000
- Fully interoperable with FireWire and i.LINK implementations of IEEE Std 1394
- Compliant with Intel *Mobile Power Guideline 2000*
- Full IEEE Std 1394a-2000 support includes: connection debounce, arbitrated short reset, multispeed concatenation, arbitration acceleration, fly-by concatenation, and port disable/suspend/resume
- Power-down features to conserve energy in battery-powered applications include: automatic device power down during suspend, PCI power management for link-layer, and inactive ports powered down
- Ultralow-power sleep mode
- Two IEEE Std 1394a-2000 fully compliant cable ports at 100M bits/s, 200M bits/s, and 400M bits/s
- Cable ports monitor line conditions for active connection to remote node
- Cable power presence monitoring
- Separate cable bias (TPBIAS) for each port
- 1.8-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments
- Physical write posting of up to three outstanding transactions
- PCI burst transfers and deep FIFOs to tolerate large host latency
- $\overline{\text{PCI\_CLKRUN}}$ protocol
- External cycle timer control for customized synchronization
- Extended resume signaling for compatibility with legacy DV components
- PHY-Link logic performs system initialization and arbitration functions
- PHY-Link encode and decode functions included for data-strobe bit level encoding
- PHY-Link incoming data resynchronized to local clock
- Low-cost 24.576-MHz crystal provides transmit and receive data at 100M bits/s, 200M bits/s, and 400M bits/s
- Node power class information signaling for system power management
- Serial ROM interface supports 2-wire serial EEPROM devices
- Two general-purpose I/Os
- Register bits give software control of contender bit, power class bits, link active control bit, and IEEE Std 1394a-2000 features
- Fabricated in advanced low-power CMOS process
- PCI and CardBus register support
- Isochronous receive dual-buffer mode
- Out-of-order pipelining for asynchronous transmit requests
- Register access fail interrupt when the PHY SCLK is not active

† Implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thompson, Limited.

- PCI power-management D0, D1, D2, and D3 power states
- Initial bandwidth available and initial channels available registers
- $\overline{\text{PME}}$ support per *1394 Open Host Controller Interface Specification*

1.3 Related Documents

- *1394 Open Host Controller Interface Specification* (Release 1.1)
- *IEEE Standard for a High Performance Serial Bus* (IEEE Std 1394-1995)
- *IEEE Standard for a High Performance Serial Bus—Amendment 1* (IEEE Std 1394a-2000)
- *PC Card Standard—Electrical Specification*
- *PC 2001 Design Guide*
- *PCI Bus Power Management Interface Specification* (Revision 1.1)
- *PCI Local Bus Specification* (Revision 2.2)
- *Mobile Power Guideline 2000*
- *Serial Bus Protocol 2* (SBP-2)
- *IEC 61883-1:1998 Consumer Audio/Video Equipment Digital Interface Part 1: General*

1.4 Trademarks

1.5 Ordering Information

ORDERING NUMBER	NAME	VOLTAGE	PACKAGE
TSB43AB22A	iOHCI-Lynx	3.3 V	PDT

Version 1.1 2007

PEX 8112

ExpressLane™ PCI Express to PCI Bridge

Features

- *General Features*
  - Forward and Reverse bridging
  - 144-ball BGA package with standard 1.0 mm pitch (13mm x 13mm)
  - 161-ball BGA package with fine 0.65 mm pitch (10mm x 10mm)
  - Low power – 400 milliwatts
  - EEPROM configuration option with SPI
  - Internal 8Kbyte shared RAM
  - 1.5 V core supply voltage
  - JTAG
  - Four (4) GPIO pins for maximum design flexibility
  - Extensive PME support including D0 and $D0_{Active}$, D1, D2 and $D3_{Hot}$ and $D3_{Cold}$
  - Leaded and Lead-free standard pitch packaging available
  - Lead-free fine pitch packaging only
  - Industrial Temperature: -40 to +85ºC
- *Integrated PCI Express Interface*
  - PCI Express Base 1.0a compliant
  - x1 Link, dual-simplex, 2.5 Gbps per direction
  - One virtual channel
  - Automatic LVDS polarity reversal
  - 128 byte maximum payload size
  - Link CRC
  - Link power management
  - Flow control buffering
  - PCI Express transaction queues for eight (8) outstanding TLPs
- *PCI Interface*
  - PCI v.3.0: 32 bits, up to 66 MHz
  - PCI Power Management 1.1
  - Internal arbiter supports up to 4 external masters; REQ#/GNT# signals
  - 3.3V I/O and 5V tolerant PCI
  - Message Signal Interrupt (MSI) support
  - Provides PCI clock output
  - Four mailbox registers for messaging
  - VGA and ISA Enable registers for legacy operation

PLX TECHNOLOGY
THE I/O INTERCONNECT SOLUTION

Reversible Bridge in a Tiny Package

The PLX Technology PEX 8112 bridge enables designers to migrate legacy PCI bus interfaces to the new advanced serial PCI Express. This is ideal for including existing PCI ICs on a PCI Express™ Adapter Board, such as the new ExpressCard™ or AdvancedMC™ standards. The 13mm x 13mm standard BGA package or 10mm x 10mm fine BGA package offerings makes the PEX 8112 bridge well suited for applications where board real estate is at a premium. With its low power 0.15 micron CMOS design, the PEX 8112 consumes only about 400 mW of power.

Forward and Reverse Bridging

The PEX 8112 supports **forward and reverse bridging** as defined by the PCI Express-to-PCI/PCI-X Bridge Specification 1.0. In forward mode, the bridge allows legacy PCI chips and adapters to be used with new PCI Express processor systems. Reverse bridge operation allows conventional PCI processors and chipsets to configure and control advanced PCI Express switches and endpoints. The reverse PEX 8112 not only allows complete configuration of a downstream PCI Express system from the PCI bus, but it also handles limited PCI Express root functions for reverse interrupt and Power Management Events.

Block Diagram

The PEX 8112 is equipped with a standard PCI Express port that operates as a single, x1 link with a maximum of 250 Megabytes per second of throughput per transmit and receive direction. The single 2.5 Gbps integrated SerDes delivers the highest bandwidth with the lowest possible pin count using LVDS technology.

The PEX 8112 has a single parallel bus segment supporting the PCI v.3.0 protocol, and a 32-bit wide parallel data path running up to 66MHz.

The device supports internal queues with flow control features to optimize throughput and traffic flow.

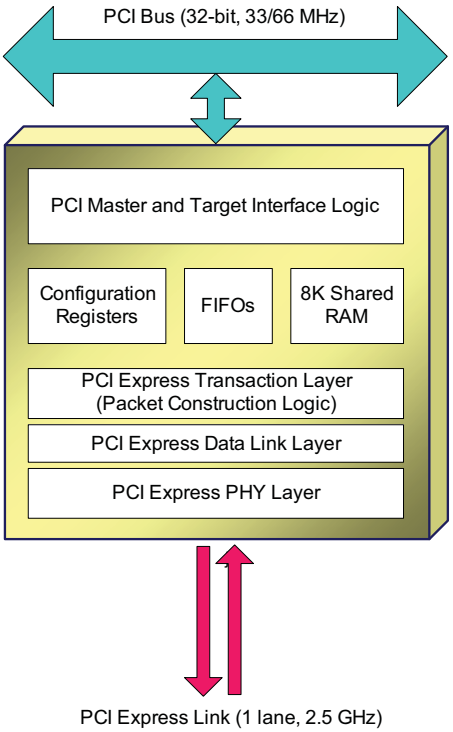


Figure 1. PEX 8112 Block Diagram