規格書
Data Sheet

CUSTOMER :

Allied Vision

Model NO :

FWB1GLC-PCIE1X10

DESCRIPTION :

3 port OHCI 1.2 Compliant Firewire 800 (IEEE 1394b) & GOF (LC-Duplex) to PCI Express Host Adapter

Revision :

1.0.3

Date: 2014/11/27

CUSTOMER APPROVED	APPROVAL	ENGINEER	ISSUE BY

IOI Technology Corporation

映奧股份有限公司

台北縣新店市寶橋路 235 巷 125 號 4 樓

4F, No.125, Lane 235, Baociao Rd, Sindian City,
Taipei County 231, Taiwan, R.O.C.

TEL : 02-89191358 FAX : 02-89191359

Content

Overview:

Introduction

FWB1GLC-PCIE1X10 is designed with Texas Instruments XIO2213B controller.

The Texas Instruments XIO2213B is a PCI Express to PCI translation bridge where the PCI bus interface is internally connected to a 1394b open host controller link-layer controller with a three-port 1394b PHY. The PCI-Express to PCI translation bridge is fully compatible with the *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The 1394b OHCI controller function is fully compatible with IEEE Standard 1394b and the latest *1394 Open Host Controller Interface (OHCI)* Specification.

Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The device provides physical write posting and a highly tuned physical data path for SBP-2 performance. The device is capable of transferring data between the PCI Express bus and the 1394 bus at 100M bits/s, 200M bits/s, 400M bits/s, and 800M bits/s.

FWB1GLC-PCIE1X10 provides full PCI Express and 1394b functionality and performance.

Technical Specifications

PCI Express

- Full x1 PCI Express Throughput
- Fully Compliant with PCI Express Base Specification, Revision 1.1
- Utilizes 100-MHz Differential PCI Express Common Reference Clock

OHCI Link and IEEE 1394 PHY

- Fully supports provisions of IEEE P1394b-2002
- Fully Compliant With Provisions of IEEE Std 1394-1995 for a High-Performance Serial Bus and IEEE Std 1394a-2000
- Fully Compliant with 1394 Open Host Controller Interface Specification, Revision 1.1 and Revision 1.2 draft
- Three IEEE Std 1394b Fully Compliant Cable Ports at 100M Bits/s, 200M Bits/s, 400M Bits/s, and 800M Bits/s
- Cable Ports Monitor Line Conditions for Active Connection To Remote Node
- Cable Power Presence Monitoring
- EEPROM Configuration Support to Load the Global Unique ID for the 1394 Fabric
- Active State Link Power Management Saves Power When Packet Activity on the PCI Express Link is Idle, Using Both L0s and L1 States
- Support for D1, D2, D3hot

Fiber Optical Port

- Supports Gigabit Ethernet 850nm VCSEL (Multi-Mode) Transceiver with LC-Duplex Connector
- Compliant with Specifications for IEEE 802.3 Gigabit Ethernet (1.25Gbd) 1000BASE-SX
- Maximum link lengths:
  - ◇ 220 m Links in **62.5/125** μm MMF 160 MHz*km Cables
  - ◇ 275 m Links in **62.5/125** μm MMF 200 MHz*km Cables
  - ◇ 500 m Links in **50/125** μm MMF 400 MHz*km Cables
  - ◇ 550 m Links in **50/125** μm MMF 500 MHz*km Cables
- Class 1 Laser International Safety Standard IEC 825 Compliant

Number of Ports

- Two Bilingual **IEEE Std 1394b-2002** Cable Ports
- One GOF (LC-Duplex) Port

Bus Power Connector

- Big IDE 4-pin DC Power Connector

Operating System Requirements

The 1394b function (host driver) is supported (built in) by the following OS:

- Windows 2000 SP4 or later
- Windows XP SP2 or later
- Windows 7, 8 and 8.1
- Mac OS 10.4 or later
- Linux kernel 2.6.23 or later.

RoHS

This Host Adapter is satisfied with RoHS regulations. Material of solder is satisfied with following definition.

	Material of solder
Solder Paste	SN-3.0AG-0.5CU
Flow and hand soldering	SN-0.7CU+NI

Environmental Condition

Operating free-air temperature: 0 ~ 65 degree C
Storage temperature range: -20 ~ 100 degree C
Humidity Operating : 0 ~ 80% RH, Non-condensing

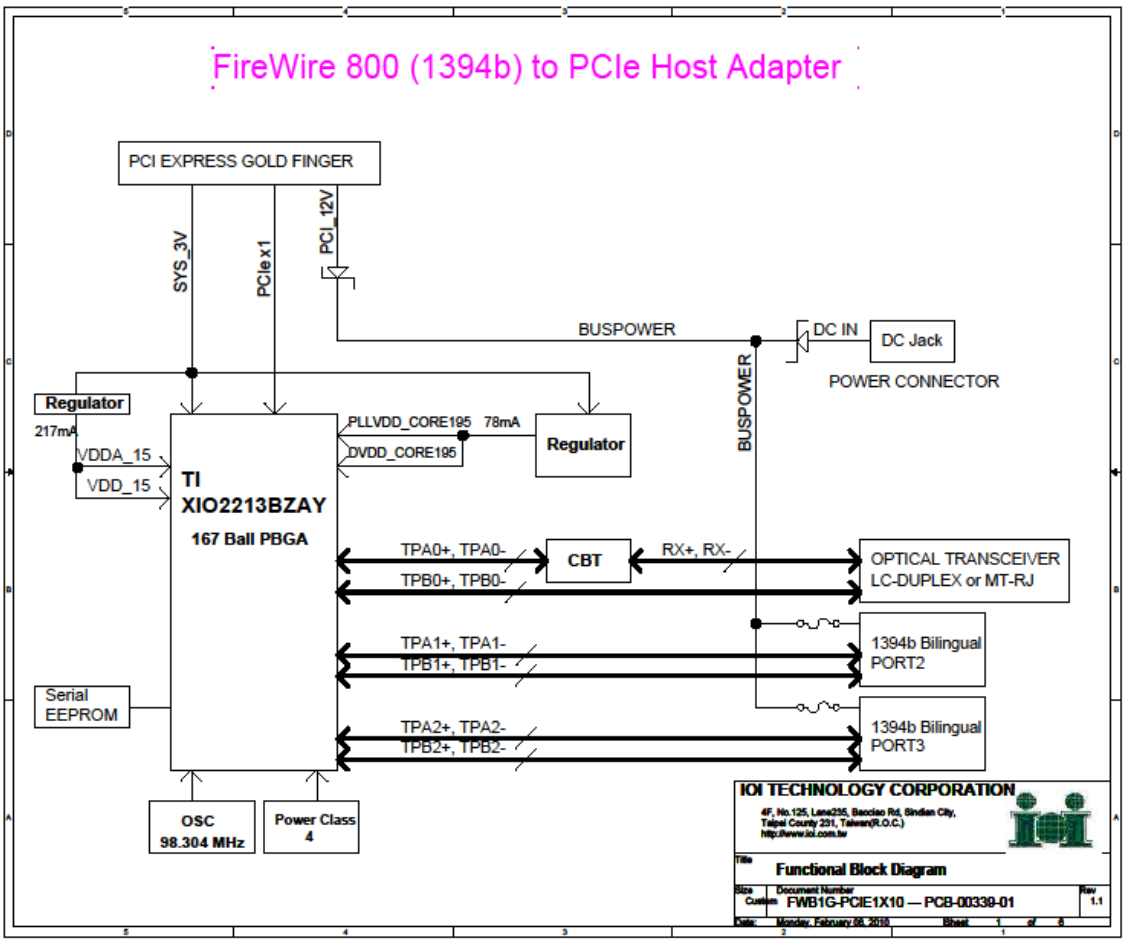
IEEE 1394 Power Class

FWB1GLC-PCIE1X10 was designed with 1394 power class 4 (PC0 ~ PC2 = 100).
The Physical layer (TSB81BA3D) of FWB1GLC-PCIE1X10 can be powered from FireWire (IEEE 1394) bus to act as a repeater.

IEEE 1394 Bus Power

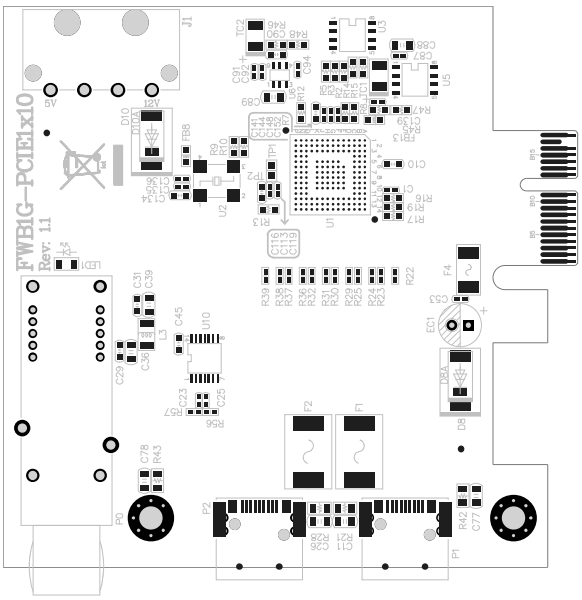
Power supply to the FireWire (IEEE 1394) bus power may from the following source
A. From PCI Express: +12V (500mA)
B. From J1: SMPS (Switching Mode Power Supply) DC +12V
C. From FireWire (IEEE 1394) Bus Power
*IEEE 1394 Bus Power (Power for the IEEE 1394 Bus): All FireWire (IEEE 1394) port is protected by one 1.5A/33V Fuse.

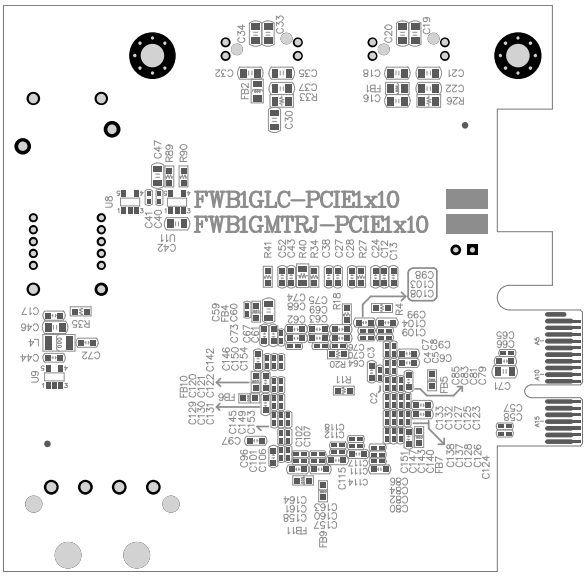
Block Diagram



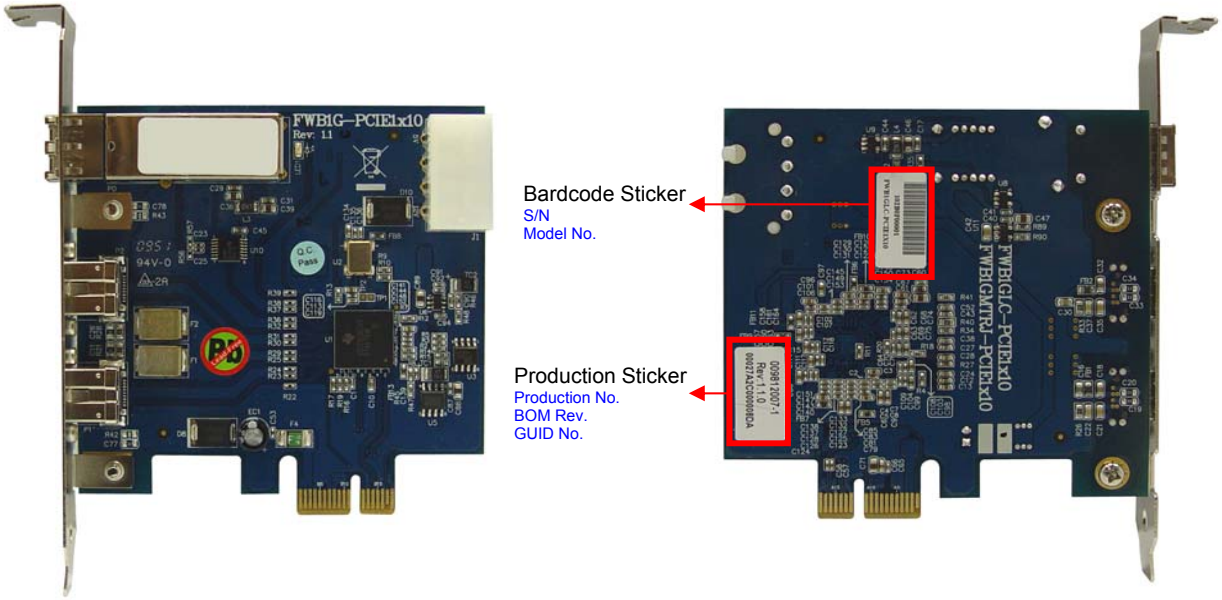
Silk Screen and Picture:

Silk Screen of FWB1G-PCIE1X10 P.C.B

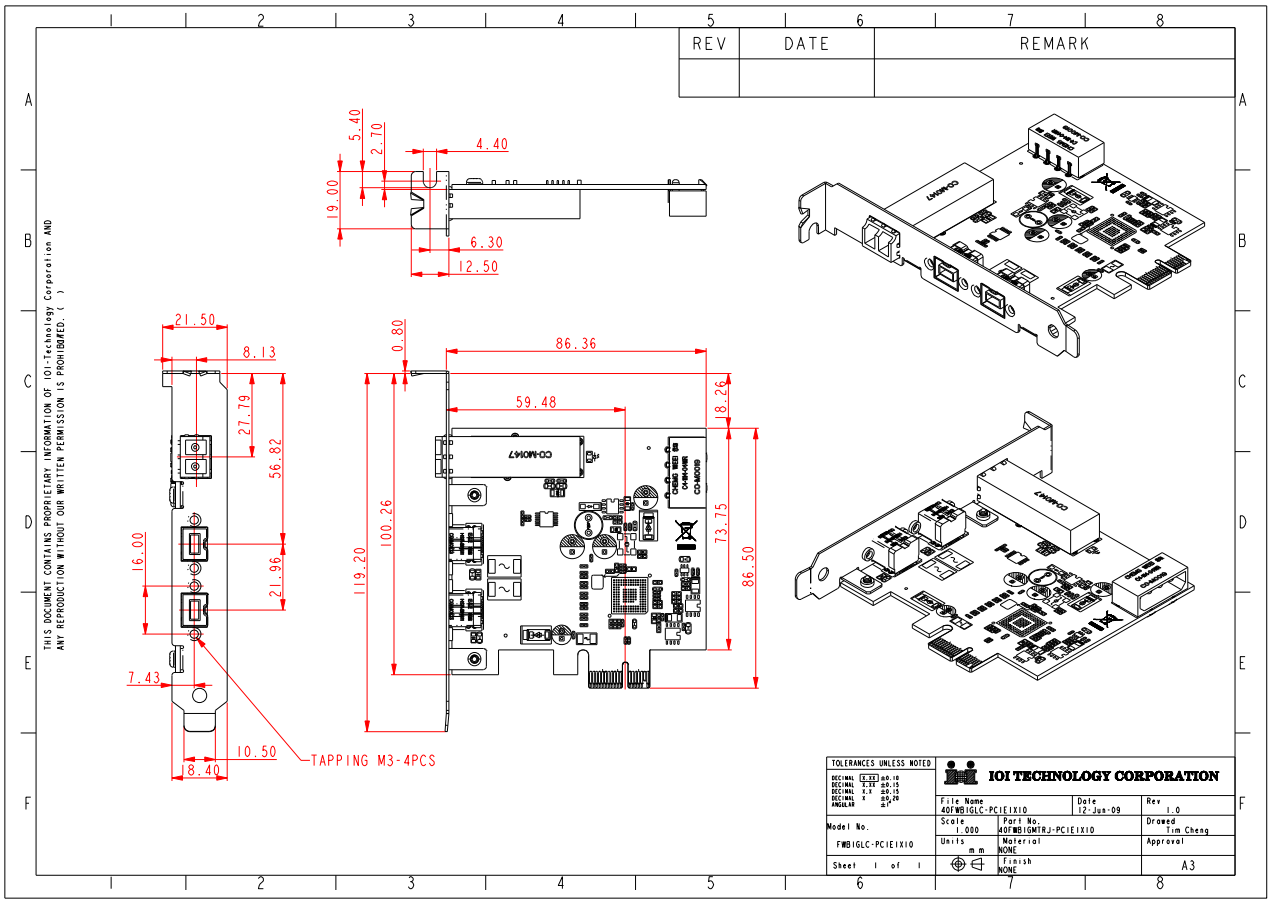




Picture of FWB1GLC-PCIE1X10

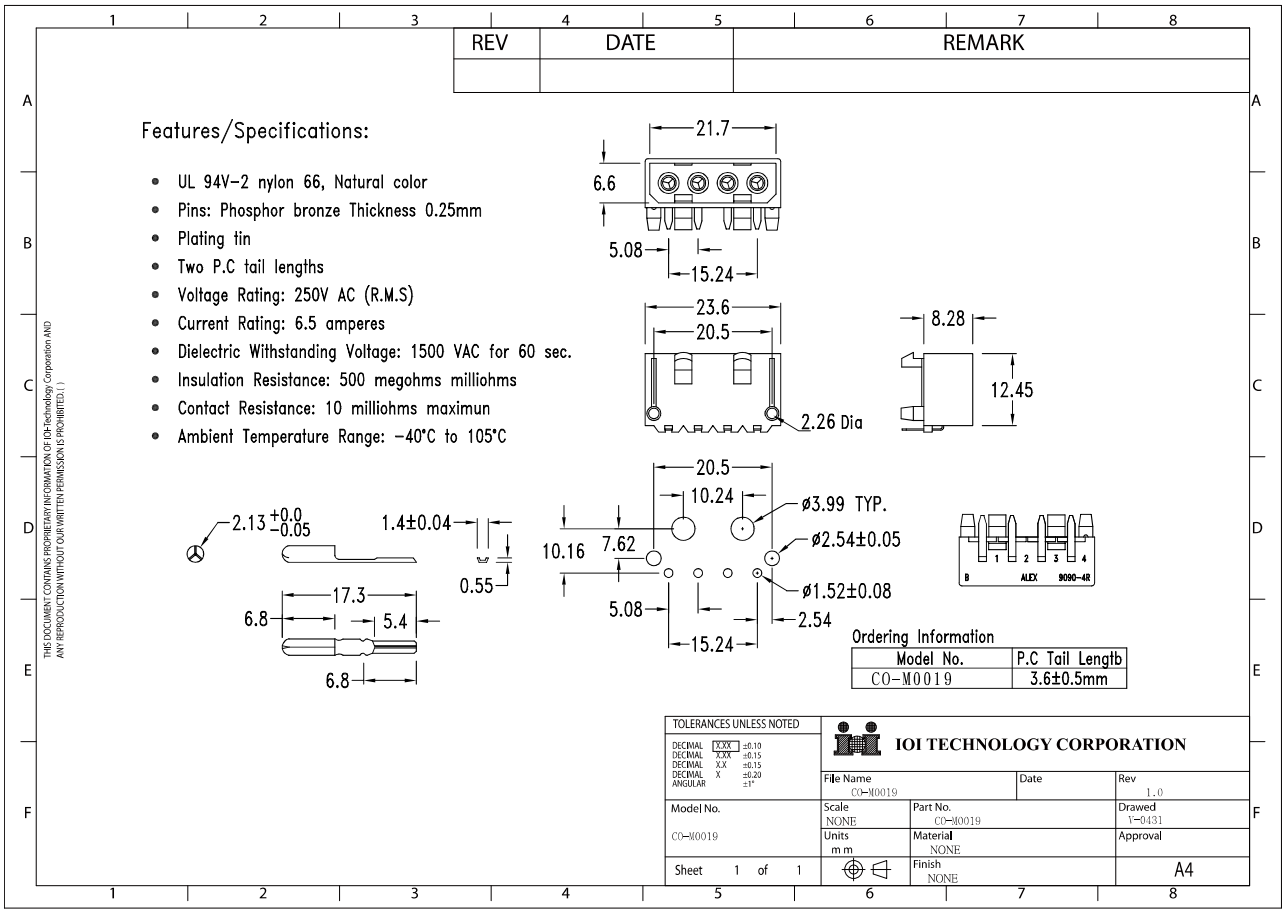


Mechanical Dimension:



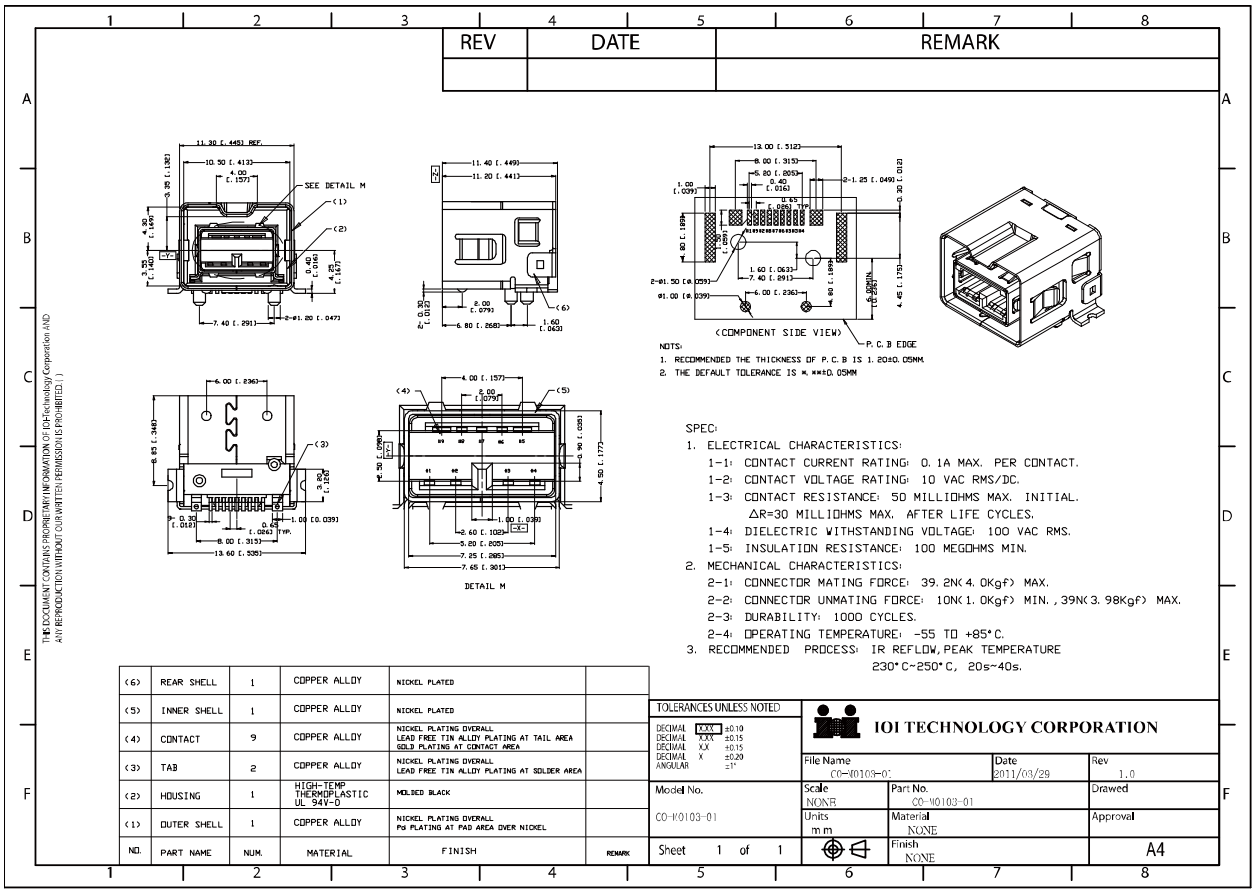
Key Parts Information:

Datasheet of Power Connector



Key Parts Information:

Datasheet of Bilingual Connector



Key Parts Information:

Datasheet of LC-Duplex Connector

CO-M0147-01
OPTICAL TRANSCEIVER, SG8512-X5ATO SANOC; 1.25Gbps 850nm VCSEL Multi-Mode Fiber Transceiver, 3.3V, LC-Duplex Connector, SFF Package

SANOC

SANOC 2x5 SFF Transceiver

SG8512-X5ATO

850nm VCSEL 1.25Gbps 3.3V Multi Mode Transceiver

Description

General

The SG8512-X5ATO transceiver from SANOC is the industry standard 2x5 package with LC duplex fiber optical connector for serial optical data communications applications specify of Gigabit Ethernet IEEE802.3z/D5 and Fiber Channel. This module is designed for multi mode fiber and operates at a nominal wavelength of 850nm VCSEL with cost effective and high performance

Transmitter Section

The transmitter consists of a high-performance 850nm Vertical Cavity Surface Emitting Laser (VCSEL) laser in the optical subassembly (OSA), which is housed within a plastic barrel package. In addition, this component is also class 1 laser compliant with according to International Safety Standard IEC-825.

Receiver Section

The receiver contain of an GaAs PIN photodiode coupled to a high sensitivity transimpedance amplifier (TIA) in an OSA. This OSA combination is mated to a post amplifier IC that provides the post amplification and SD (Signal Detect) indication circuit, which provides LVTTL logic low state output when an unusable input optical signal level is detected.

Features

- Single + 3.3 V Power Supply
- Compliant with Specification for IEEE802.3z / D5
- Compliant with Specification for Fiber Channel
- Multimode Fiber, LC Duplex Interface
- Class 1 Laser International Safety Standard IEC 825 Compliant
- Low Power Consumption
- Temperature Range : 0℃ to +70℃
- RoHS Compliant

Applications

- Bridges/Routers/intelligent hub and concentrators
- Gigabit Ethernet / Fiber Channel
- Storage Area Network

Performance Specifications

Absolute Maximum Ratings					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply Voltage	V_{CC}	0	-	5	V
Storage Temperature	T_S	-40	-	85	℃
Operating Temperature	T_{OP}	0	-	70	℃
Lead Soldering Limits	T_{SOLD}	-	-	260	℃/sec
General Specifications					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Data Rate	B	-	1.25	-	Gbps
Supported Link Length on 62.5/125μm MMF	L	-	0.5	-	Km

Key Parts Information:

Datasheet of Integrated Circuit

1 Introduction

1.1 XIO2213B Features

- Full ×1 PCI Express™ (PCIe) Throughput
- Fully Compliant With PCI Express Base Specification, Revision 1.1
- Utilizes 100-MHz Differential PCI Express Common Reference Clock or 125-MHz Single-Ended Reference Clock
- Fully Supports Provisions of IEEE Std P1394b-2002
- Fully Compliant With Provisions of IEEE Std 1394-1995 for a High-Performance Serial Bus and IEEE Std 1394a-2000
- Fully Compliant With 1394 Open Host Controller Interface (OHCI) Specification, Revision 1.1 and Revision 1.2 Draft
- Three IEEE Std 1394b Fully Compliant Cable Ports at 100M Bit/s, 200M Bit/s, 400M Bit/s, and 800M Bit/s
- Cable Ports Monitor Line Conditions for Active Connection to Remote Node
- Cable Power Presence Monitoring
- EEPROM Configuration Support to Load Global Unique ID for 1394 Fabric
- Support for D1, D2, $D3_{hot}$
- Active-State Link Power Management Saves Power When Packet Activity on the PCI Express Link Is Idle, Using Both L0s and L1 States
- Eight 3.3-V Multifunction General-Purpose I/O (GPIO) Terminals

2 Overview

The Texas Instruments XIO2213B is a single-function PCI Express™ (PCIe) to PCI local bus translation bridge, where the PCI bus interface is internally connected to a 1394b open host controller/link-layer controller with a 3-port 1394b physical layer (PHY). When the XIO2213B is properly configured, this solution provides full PCIe and 1394b functionality and performance.

2.1 Description

The TI XIO2213B is a PCIe to PCI translation bridge, where the PCI bus interface is internally connected to a 1394b open host controller/link-layer controller with a 3-port 1394b PHY. The PCIe to PCI translation bridge is fully compatible with the PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The 1394b OHCI controller function is fully compatible with IEEE Std 1394b and the latest 1394 Open Host Controller Interface (OHCI) Specification.

The XIO2213B simultaneously supports up to four posted write transactions, four nonposted transactions, and four completion transactions pending in each direction at any time. Each posted write data queue and completion data queue can store up to 8K bytes of data. The nonposted data queues can store up to 128 bytes of data.

The PCIe interface supports a x1 link operating at full 250 Mbit/s packet throughput in each direction simultaneously. Also, the bridge supports the advanced error reporting capability including ECRC as defined in the PCI Express Base Specification, Revision 1.1. Supplemental firmware or software is required to fully utilize both of these features.

Robust pipeline architecture is implemented to minimize system latency. If parity errors are detected, packet poisoning is supported for both upstream and downstream operations.

PCIe power management (PM) features include active-state link PM, PME mechanisms, and all conventional PCI D states. If the active-state link PM is enabled, the link automatically saves power when idle using the L0s and L1 states. PM active-state NAK, PM PME, and PME-to-ACK messages are supported. The bridge is compliant with the latest PCI Bus Power Management Specification and provides several low-power modes, which enable the host power system to further reduce power consumption

Eight general-purpose inputs and outputs (GPIOs), configured through accesses to the PCIe configuration space, allow for further system control and customization.

Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The device provides physical write posting and a highly tuned physical data path for SBP-2 performance. The device is capable of transferring data between the PCIe bus and the 1394 bus at 100M bit/s, 200M bit/s, 400M bit/s, and 800M bit/s. The device provides three 1394 ports that have separate cable bias (TPBIAS).

As required by the 1394 Open Host Controller Interface (OHCI) Specification, internal control registers are memory mapped and nonprefetchable. This configuration header is accessed through configuration cycles specified by PCIe, and it provides plug-and-play (PnP) compatibility.

The PHY provides the digital and analog transceiver functions needed to implement a 3-port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. An optional external 2-wire serial EEPROM interface is provided to load the global unique ID for the 1394 fabric.

The XIO2213B requires an external 98.304-MHz crystal oscillator to generate a reference clock. The external clock drives an internal phase-locked loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL. Data bits to be transmitted through the cable ports are latched internally, combined serially, encoded, and transmitted at 98.304, 196.608, 393.216, 491.52, or 983.04 Mbit/s (referred to as S100, S200, S400, S400B, or S800 speed, respectively) as the outbound information stream.

To ensure that the XIO2213B conforms to IEEE Std 1394b-2002, the BMODE terminal must be asserted. The BMODE terminal does not select the cable-interface mode of operation. BMODE selects the internal PHY-section/LLC-section interface mode of operation and affects the arbitration modes on the cable. BMODE must be pulled high during normal operation.

Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They can be pulled high through a 1-k? resistor or hardwired low as a function of the equipment design. The PC0, PC1, and PC2 terminals indicate the default power class status for the node (the need for power from the cable or the ability to supply power to the cable). The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the XIO2213B, this bit can only be set by a write to the PHY register set. If a node is to be a contender for IRM or BM, the node software must set this bit in the PHY register set.